CLAIMS

1. Phase lock loop, comprising a controlled oscillator (30) to deliver a high frequency signal (S), a frequency divider (31) to convert the high frequency signal into a divided frequency signal (QA), a phase comparator (32) to receive the divided frequency signal and a reference signal (FREF) and produce a signal (INVP, INVN) measuring a phase difference between the divided frequency signal and the reference signal, and a low-pass filter (34) to control the oscillator on the basis of the measurement signal,
characterized in that it also comprises means (35) for generating a measurement window, of a duration (L) defined by counting cycles of the high frequency signal, in response to each active edge of the divided frequency signal,
and in that the phase comparator is built to activate the measurement signal during the measurement window in response to each active edge of the divided frequency signal, so that the measurement signal comprises, when an active edge of the reference signal falls within the measurement window, a first pulse between the start of the measurement window and said active edge of the reference signal and a second pulse opposite to the first pulse between said active edge of the reference signal and the end of the measurement window.

2. Phase lock loop according to Claim 1, characterized in that the phase comparator is designed to produce the measurement signal in the form of two components (INVN, INVP), each having a respective activation duration, the difference between said activation durations of the components being a piecewise linear function of a time offset between the divided frequency signal

(QA) and the reference signal (FREF).

3. Phase lock loop according to Claim 1 or 2, wherein the means for generating the measurement window comprise means (35) of producing a replica (QB) of the divided frequency signal (QA), reproducing each active edge of the divided frequency signal with a delay generated from the high frequency signal (S).

4. Phase lock loop according to any one of the preceding claims, wherein the duration (L) of the measurement window is a whole number of cycles of the high frequency signal (S).

5. Phase lock loop according to any one of the preceding claims, comprising a charge pump (33) to inject a first current at a node (55) of the low-pass filter (34) in response to the first pulse (INVN) of the measurement signal and to inject a second current, opposite to the first current and of the same intensity (I_P), at said node of the low-pass filter in response to the second pulse (INVP) of the measurement signal.

6. Phase lock loop according to Claim 5, wherein the charge pump (33) comprises two substantially identical current generators (50, 60) to generate the first and second currents.

7. Phase lock loop according to Claim 6, wherein the two current generators (50, 60) produce a digitally adjustable current intensity (I_P).

8. Phase lock loop according to Claim 7, comprising means for varying said adjustable intensity (I_P) according to a division factor (P) applied by the frequency divider (31).

9. Phase lock loop according to Claim 7 or 8, comprising means for giving said adjustable intensity (I_P) a higher value in a frequency locking search step of the loop than in a phase tracking step executed after frequency locking.

10. Phase lock loop according to any one of Claims 5 to 8, wherein the charge pump (33) comprises a switch bridge having a first path including two switches in series (51, 52) respectively controlled by two components (INVP, INVN) of the measurement signal carrying the first and second pulses, and a second path including two other switches in series (53, 54) respectively controlled by the logical complements of said components of the measurement signal, said node (55) of the low-pass filter (34) being situated between the two switches in series of the first path.

11. Phase lock loop according to Claim 9, wherein the charge pump (33) also comprises a recopy amplifier (58) having an input linked to said node (55) of the low-pass filter (34) and an output connected to a node (56) of the switch bridge situated between the two switches in series (53, 54) of the second path and to a capacitive element (57).

12. Phase lock loop according to any one of the preceding claims, in which the phase comparator (32) comprises:

- a phase difference detection logic circuit (10) receiving the divided frequency signal (QA) and the reference signal (FREF), and delivering on the one hand a first detection signal (D) activated, after an active edge of the reference signal preceding an active edge of the divided frequency signal, during a period corresponding to the time interval between said active edges,

and on the other hand a second detection signal (U) activated, after an active edge of the divided frequency signal preceding an active edge of the reference signal, during a period corresponding to the time interval between said active edges;

- a pulse signal generator (100), producing a pulse signal (PR) active during the measurement window;
- means (111-114) for producing a separation signal (W) changing from a first level to a second level with a fixed delay in response to an active edge of the reference signal; and
- a charge transfer control logic circuit (120) combining at least the detection signals, the separation signal and said pulse signal, and producing two components (INVN, INVP) of the measurement signal, respectively carrying said first and second pulses, such that, while said pulse signal (PR) is active, one of the two components (INVN) presents the first pulse if the separation signal (W) is at the first level, and the other one of the two components (INVP) presents the second pulse if the separation signal (W) is at the second level.